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ARTICLE

Electronic Properties of $MoSe_2/ZrSe_3$ Junction Field Effect Transistor

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ABSTRACT: Transition metal dichalcogenides (TMDs) and transition metal trichalcogenides (TMTCs) exhibit tunable electronic properties, and when stacked together in their two dimensional (2D) forms, they can display distinctive electronic properties beyond those of conventional heterostructures. In this study, we fabricated for the first time junction field effect transistor (JFET) by stacking $MoSe_2$, a transition metal dichalcogenide (TMD), with $ZrSe_3$, a transition metal trichalcogenide (TMTC). We characterized its electrical properties, where the device's electrical characteristics were analyzed based on the stacking sequence. Two device configurations top-gate and bottom-gate JFETs were fabricated and systematically analyzed. Notably, the top-gate JFET exhibited superior performance, with transconductance (gm) reaching 12.8 μS, carrier mobility up to 366.95 cm^2/Vs, and a subthreshold swing (SS) of 13.25 V/dec, significantly outperforming the bottom-gate configuration. The successful demonstration of this device not only establishes the feasibility of $MoSe_2/ZrSe_3$ heterojunctions for high performance JFET applications but also paves the way for next generation electronic devices based on engineered 2D heterostructures.

KEYWORDS: Transition metal dichalcogenides (TMDs); transition metal trichalcogenides (TMTCs); molybdenum diselenide ($MoSe_2$); zirconium triselenide ($ZrSe_3$); junction field effect transistor (JFET)

1 Introduction

With the recent advances in next generation semiconductor technologies and the development of ultraminiaturized electronic devices, extensive research is underway to explore alternative materials that can overcome the physical limitations of conventional silicon based semiconductors. As a strategy to address these limitations, the introduction of new materials and the innovation of device architectures have emerged as key directions. Among these, two dimensional materials, including graphene, have garnered significant attention as promising candidates due to their atomic scale thinness and excellent electrical, optical, and mechanical properties [1–5]. In particular, 2D materials have been actively studied for their applications in various electronic and optoelectronic devices, such as transistors [6–14], memory devices, photodetectors, sensors, bioelectronics, and wearable devices [15–17]. Furthermore, vertical heterostructures formed by stacking different 2D materials exhibit unique electrical and optical properties that are difficult to achieve with conventional materials [18–23].

Graphene is well known for its exceptional electrical and mechanical properties; however, its lack of a bandgap limits its applicability in many device architectures [24]. TMDs, which are representative 2D semiconductors composed of transition metals and chalcogen elements, offer high carrier mobility, tunable bandgaps, and excellent optoelectronic properties, making them well suited for a wide range of electronic and optoelectronic applications. $MoSe_2$, a well known TMDs material, exhibits outstanding electrical and optical characteristics and has been considered a strong candidate for such applications [25–28]. On the other hand, TMTCs, which possess unique electronic properties similar to TMDs, have recently gained attention. Among them, $ZrSe_3$ is a promising quasi-one-dimensional TMTC that crystallizes in a monoclinic $P2_1/m$ structure. Each Zr atom is coordinated by eight Se atoms in a distorted bicapped trigonal-prismatic configuration, forming anisotropic chain-like layers. This characteristic crystal structure gives rise to strong in-plane optical and electrical anisotropy, as previously reported [29–31]. Notably, $ZrSe_3$ exhibits quasi one dimensional charge transport characteristics, providing novel possibilities for electronic and optoelectronic applications beyond conventional TMDs [32,33].

In this study, we report, for the first time, the fabrication of a heterojunction field effect transistor based on $MoSe_2$ and $ZrSe_3$. Ultrathin flakes of both materials were mechanically exfoliated and stacked so that $MoSe_2$ encapsulated $ZrSe_3$. Each semiconductor acts as both the channel and gate for the other, resulting in a unique mutual gating geometry that exhibits strong junction field effect transistor (JFET) behavior. This configuration enables direct modulation of interfacial transport and marks the first demonstration of a $MoSe_2/ZrSe_3$ JFET, offering a new platform for exploring interfacial phenomena in 2D heterostructure devices.

2 Materials and Methods

Bulk $MoSe_2$ and $ZrSe_3$ were purchased from HQ Graphene (Carrier density of $ZrSe_3$ is 1.084×10^{13} cm^{-3} and $MoSe_2$ is 1×1015 cm^{-3}). $MoSe_2$ and $ZrSe_3$ flakes were mechanically exfoliated and transferred onto a SiO_2/p-Si substrate with four predeposited titanium contacts using thermal evaporation. Atomic force microscopy (AFM) images were acquired using the Park NX20 system, and the Raman spectra of the materials were obtained using the MRS-5100 system. The electrical characteristics of the fabricated devices were analyzed using a Keithley 4200-SCS semiconductor parameter analyzer.

3 Results and Discussion

Fig. 1 shows the AFM image and height profile of the fabricated JFET device. Fig. 1a presents the 3D image measured by AFM, and Lines 1 to 3 indicate the measurement positions of $ZrSe_3$, $MoSe_2$ (Layer 1), and $MoSe_2$ (Layer 2), respectively. The fabricated device was stacked in the order of $MoSe_2$ (Layer 1)/$ZrSe_3$/$MoSe_2$ (Layer 2). Fig. 1b–d shows the thicknesses of the two dimensional materials obtained from height profiles measured along the red and green lines. The $ZrSe_3$ layer exhibits a thickness of approximately 170 nm, while the $MoSe_2$ layers (Layer 1 and 2) show thicknesses of approximately 40 nm and 35 nm, respectively.

Fig. 2 shows the Raman spectra of the $Mose_2/ZrSe_3$ device. Fig. 2a presents an optical microscope image of the fabricated device, where points 1 and 2 correspond to $MoSe_2$, while point 3 corresponds to $ZrSe_3$. Points 1 and 2 show peaks at 250 cm^{-1} (Fig. 2b) and 249 cm^{-1} (Fig. 2c), respectively, which correspond to A1g mode in the multilayered $MoSe_2$ In addition, the peak near 527 cm^{-1} observed in Fig. 2c originates from the crystalline Si substrate. As shown in Fig. 2d, $ZrSe_3$ exhibits three characteristic Raman peaks at 185, 241, and 308 cm^{-1}, which correspond to the A5g, A6g, and A8g vibrational modes, respectively. A5g and A6g modes are attributed to out of plane vibrations, while the A8g mode is associated with in-plane vibrations.

Fig. 3a shows an optical microscope image of the fabricated device. The device was deposited sequentially in the order of $MoSe_2$ (referred as layer 1 or L1), $ZrSe_3$, and $MoSe_2$ (referred as layer 2 or L2).

Fig. 3b shows the schematic diagram of the fabricated JFET structure. JFET device was deposited in the order of $MoSe_2$ (L1), $ZrSe_3$, and $MoSe_2$ (L2) on a wafer on which titanium was deposited as an electrode. Fig. 3c,d shows the current-voltage (I–V) characteristics of $MoSe_2$ and $ZrSe_3$, respectively. The insets in Fig. 3c,d shows the measurement configurations. I–V characteristics show nonlinear behavior, suggesting the presence of Schottky junction [34]. Moreover, $MoSe_2$ I–V characteristic showed lower current caused by the higher resistivity originated from the mechanical contact between layer 1 and layer 2.

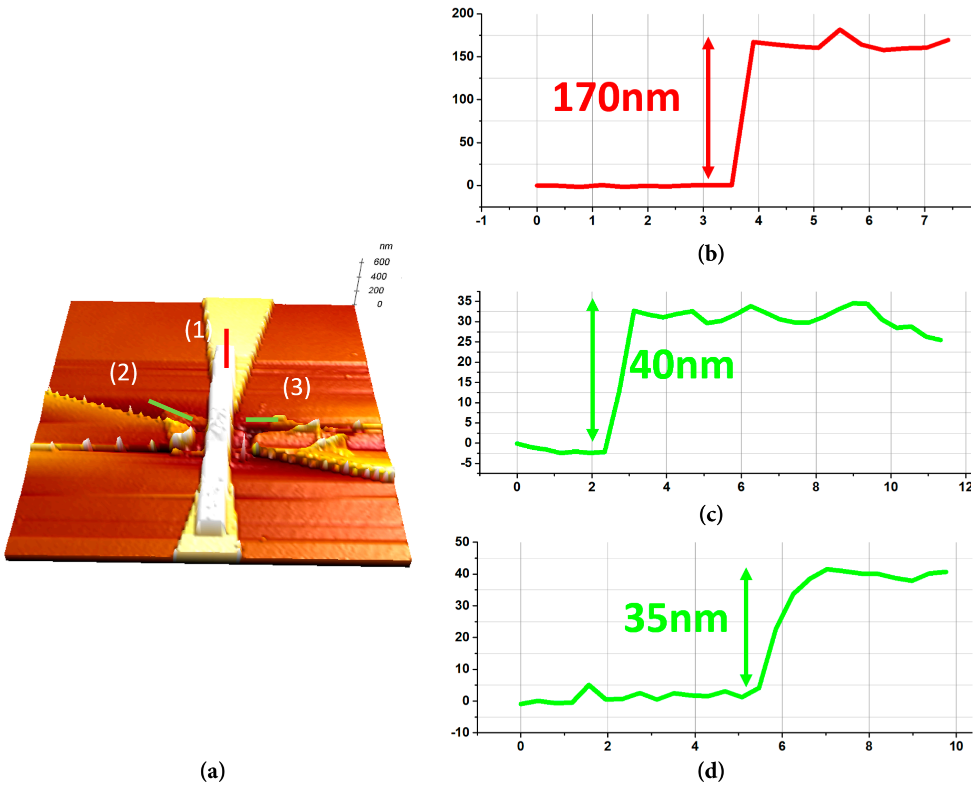

Figure 1: AFM characterization of the fabricated $MoSe_2/ZrSe_3$ JFET device. (**a**) AFM 3D image of the device and (**b**–**d**) Height profiles of $MoSe_2$ and $ZrSe_3$ layers along the marked lines.

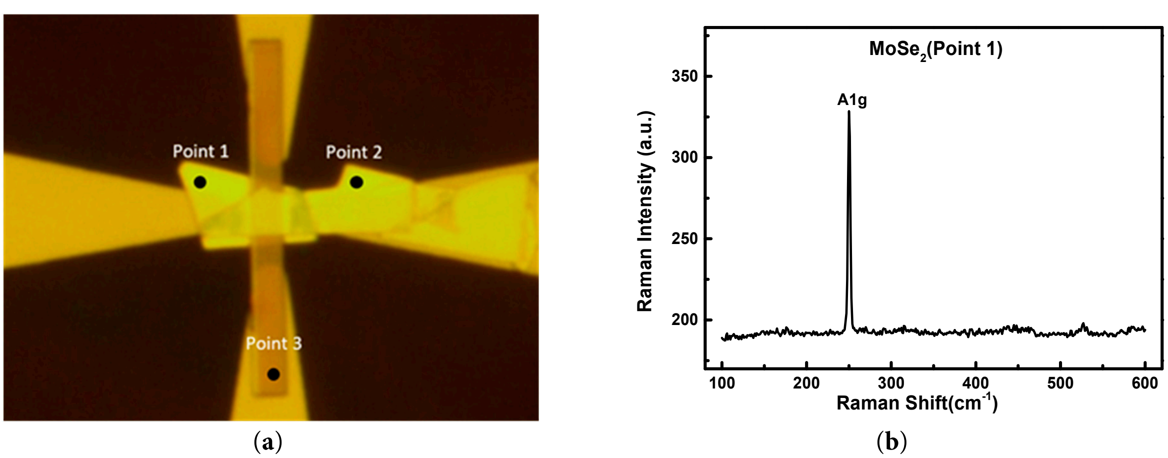

Figure 2: *Cont.*

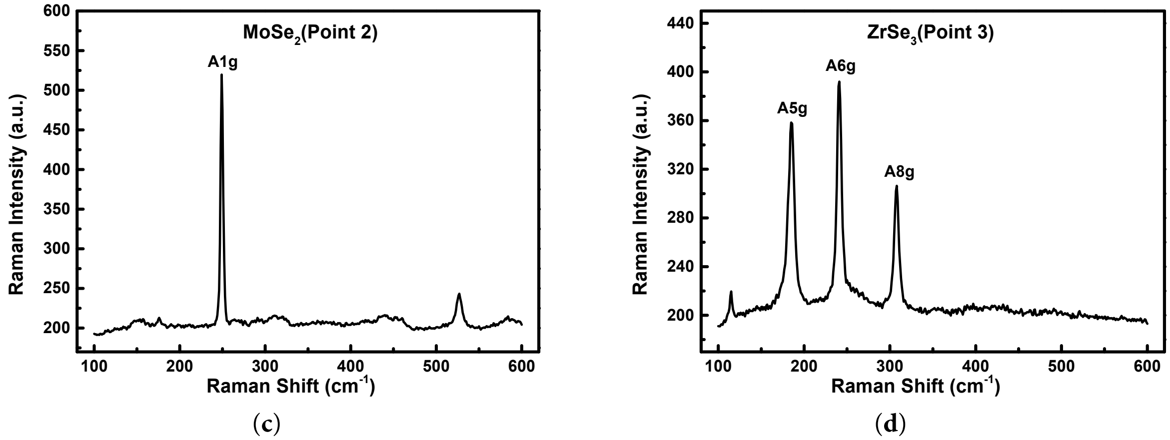

Figure 2: Raman characterization of the fabricated $MoSe_2/ZrSe_3$ heterostructure device. (**a**) shows an image of fabricated device (**b–d**) show Raman spectroscopy of $MoSe_2/ZrSe_3$ device (points 1 and 2 referenced to $MoSe_2$ layer 1 and layer 2, respectively, and point 3 referenced $ZrSe_3$).

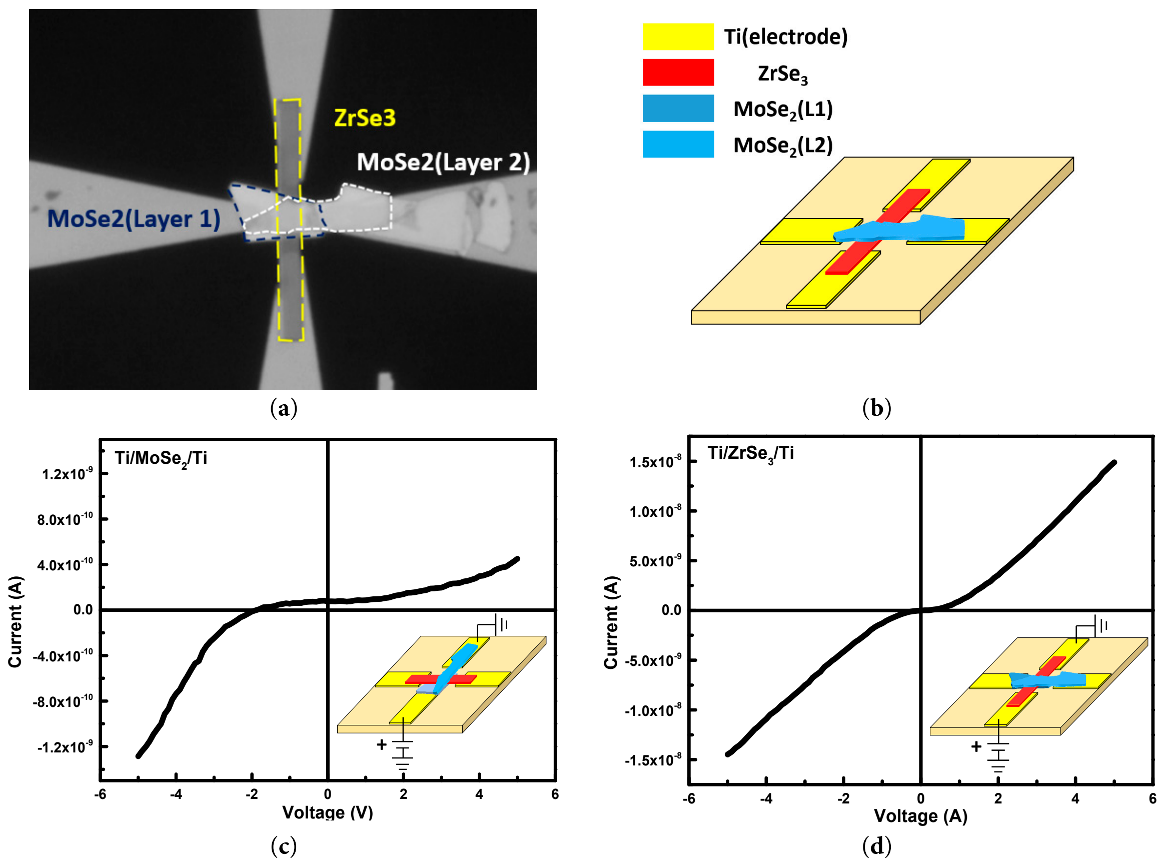

Figure 3: Device structure and electrical characterization of the $MoSe_2/ZrSe_3$ heterostructure. (**a**) Optical microscope image of device; (**b**) illustrates schematic image of the device; (**c**) I–V characteristics of Ti/$MoSe_2$/Ti; (**d**) I–V characteristics of Ti/$ZrSe_3$/Ti.

Fig. 4 is the band diagram structures of the $MoSe_2/ZrSe_3$ junction before and after contact. In the Before Contact state, each material has its own independent energy levels, with the conduction band minimum of

$MoSe_2$ located at approximately −4.6 eV [35–37], and that of $ZrSe_3$ at about −5.1 eV. The bandgap of $MoSe_2$ is around 1.1 eV, while $ZrSe_3$'s bandgap is approximately 1.55 eV, both exhibiting characteristic energy level features of TMDs and TMTCs. The work function of $ZrSe_3$ was chosen to be 5.6 eV within the typical range (5.5–5.8 eV) for quasi 1D TMTC materials owing to strong interlayer coupling and distinctive charge distribution inherent to quasi 1D TMTCs [30,38]. The valence band maximum was determined to lie at 4.6 eV relative to the vacuum level by aligning Fermi levels and incorporating experimentally measured bandgaps (1.10 eV indirect, 1.47 eV direct) [31,39]. These values agree with GW calculated bandgaps of about 1.63 eV. After contact, the Fermi levels of the two materials are aligned, which induces band bending near the hetero interface. This interfacial band modulation changes the carrier transport across the junction and affects the gating behavior of the device. In the present work, the electrical characteristics of the $ZrSe_3/MoSe_2$ top gate and bottom gate devices show p-type transfer behavior, indicating that the dominant transport in these configurations is governed by hole conduction in the $ZrSe_3$ channel.

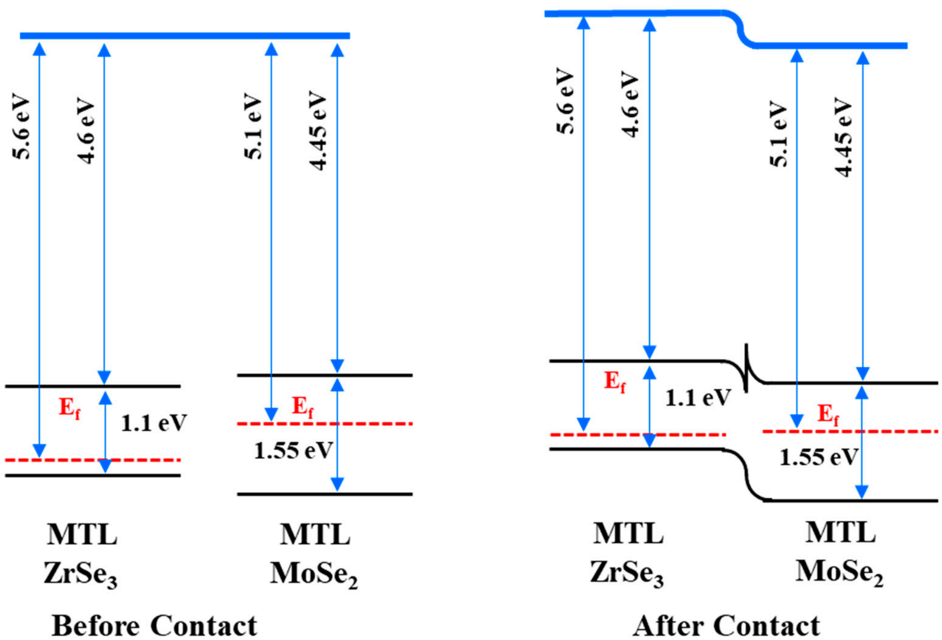

Figure 4: Energy band structure of $MoSe_2/ZrSe_3$ JFET junction before and after contact.

Fig. 5 shows the electrical characteristics of the fabricated JFET with $MoSe_2$ as the channel material. Fig. 5a illustrates a schematic of the JFET structure, highlighting the gate, source, and drain configuration. As the gate voltage increases, the energy barrier for electron injection is reduced, leading to enhanced current conduction. This modulation of the barrier height explains the n-type behavior observed in the transfer characteristics. Fig. 5b shows the drain current as a function of gate voltage for the $MoSe_2/ZrSe_3$ junction, confirming n-type behavior. The transconductance (g_m) was extracted using the relation:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (1)$$

where I_D is the drain current and V_{GS} is the gate to source voltage. Fig. 5c shows the drain voltage–drain current characteristics of the fabricated device, demonstrating n-type behavior as the drain current increases with increasing gate voltage.

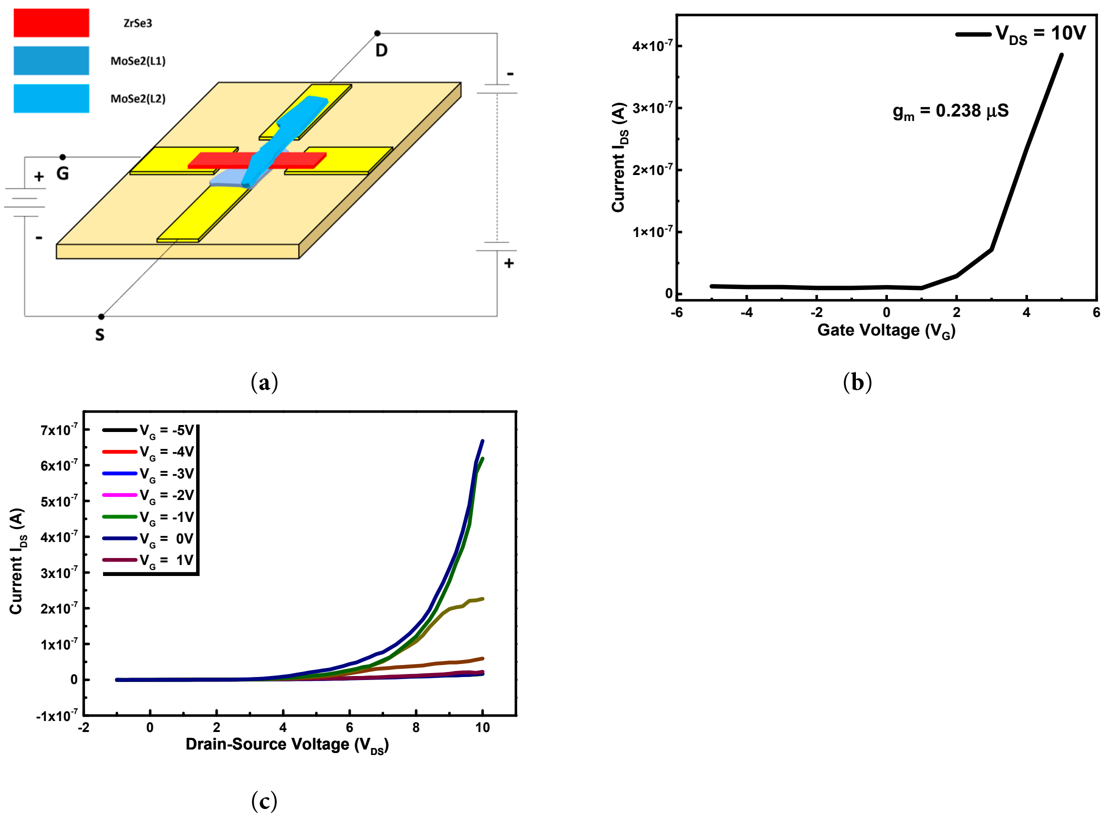

Figure 5: Electrical characteristics of the $MoSe_2$-channel $MoSe_2/ZrSe_3$ JFET. (**a**) illustrate schematic images of the $MoSe_2/ZrSe_3$ JFET. (**b**,**c**) each shows the characteristics of the fabricated $MoSe_2/ZrSe_3$ JFET.

Fig. 6 shows the electrical characteristics of the fabricated JFET. Fig. 6a illustrates a schematic of the JFET structure, highlighting the gate, source, and drain configuration. In this structure, Layer 2 $MoSe_2$ serves as the top gate. At a constant gate voltage, the carrier is moved from the source to the drain, or at a gate voltage below a certain level, the movement of the carrier is blocked by a potential barrier due to an increase in the depletion layer region [39–41]. The current due to the movement of this carrier can be confirmed in the graphs of Fig. 6. Fig. 6b shows the drain current as a function of top gate voltage for the $MoSe_2$, $ZrSe_3$ junction, confirming p-type behavior. Fig. 6c shows the drain current under varying drain voltages, where the current increases as the gate voltage decreases.

Fig. 7 shows the electrical characteristics of the fabricated JFET. Fig. 7a illustrates a schematic of the JFET structure with labeled gate, source, and drain, where Layer 1 $MoSe_2$ is used as the bottom gate. Fig. 7b shows the drain current as a function of bottomgate voltage for the $MoSe_2/ZrSe_3$ junction, confirming p-type behavior. Fig. 7c shows the drain current under varying drain voltages, where the current increases as the gate voltage decreases.

Fig. 8 represents a comparison of the electrical performance between the top gate and bottom gate configurations. A comparative analysis of gm values indicates that the top gate configuration exhibits superior transconductance characteristics relative to the bottom gate structure. This enhancement is attributed not merely to differences in surface defect induced trapping effects, but more significantly to the increased contact area and reduced contact resistance at the $MoSe_2/ZrSe_3$ interface in the top gate architecture.

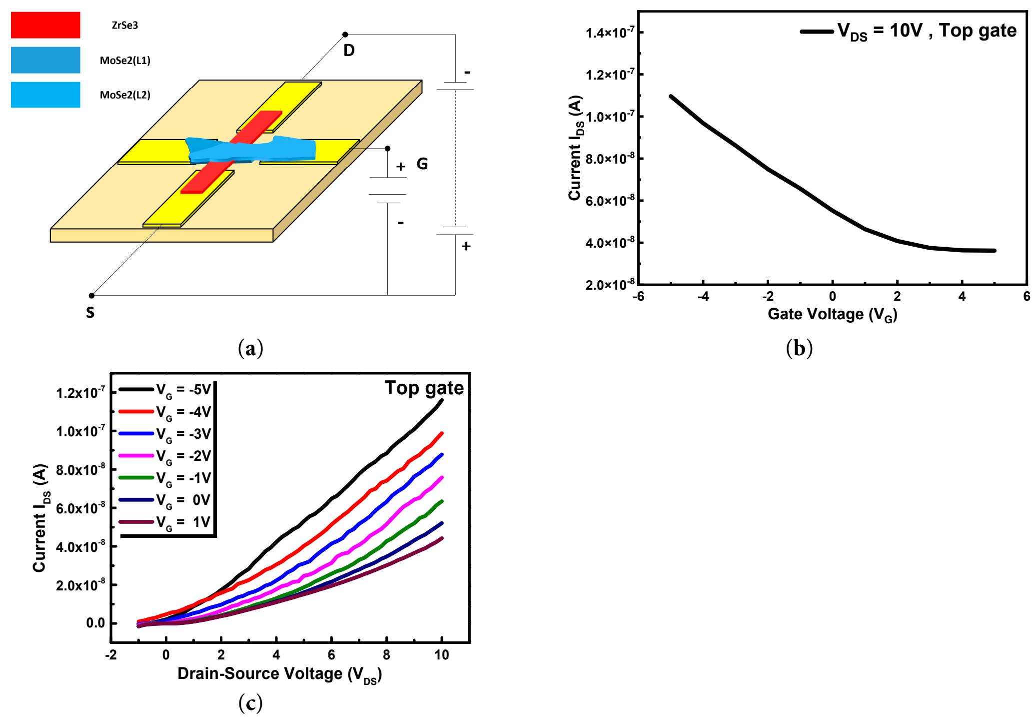

Figure 6: Electrical characteristics of the top gate $MoSe_2/ZrSe_3$ JFET. (**a**) illustrates schematic images of the $MoSe_2/ZrSe_3$ JFET. (**b**,**c**) each shows the characteristics of the fabricated top gate $MoSe_2/ZrSe_3$ JFET.

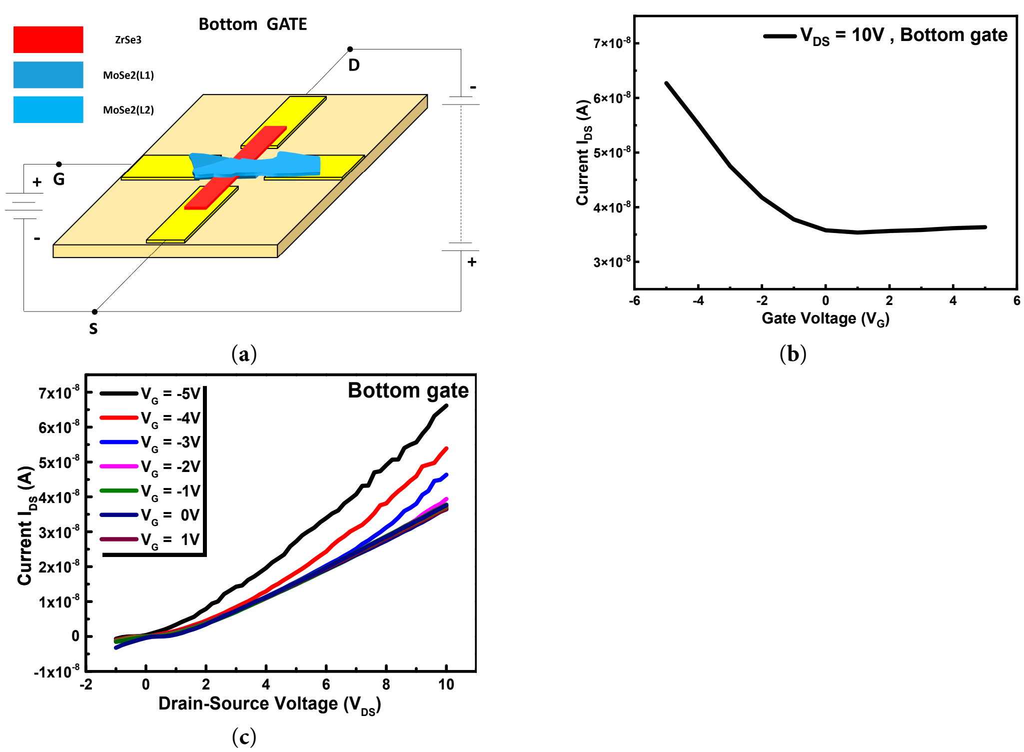

Figure 7: Electrical characteristics of the bottom gate $MoSe_2/ZrSe_3$ JFET. (**a**) illustrates schematic images of the $MoSe_2/ZrSe_3$ JFET. (**b**,**c**) each shows the characteristics of the fabricated bottom gate $MoSe_2/ZrSe_3$ JFET.

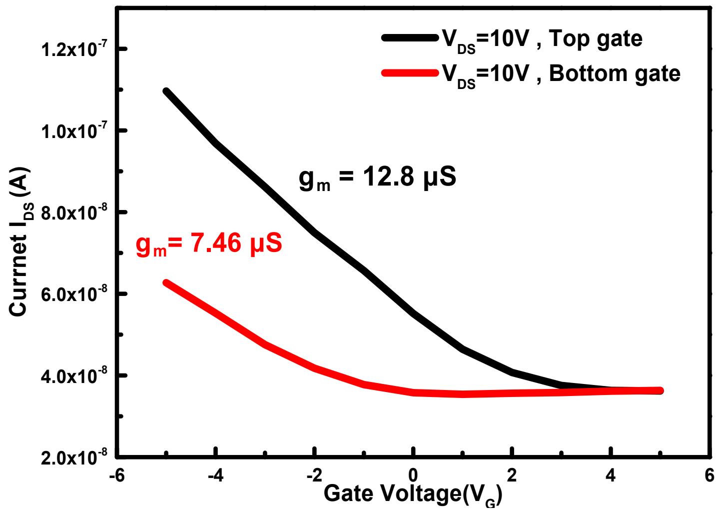

Figure 8: Compares the transconductance in top gated and bottom gated $MoSe_2/ZrSe_3$ JFETs.

Table 1 shows the g_m, mobility, and SS values of each device, as previously described. The mobility of each device was calculated using the following equations.

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{qN_d \mu t W}{L} \tag{2}$$

$$\text{Mobility}(\mu) = \frac{L g_m}{qN_d t W} \tag{3}$$

where N_d is carrier density as number per cm^3; q is an electronic charge; and t, W, and L are the thickness, width, and length of the channel [42,43].

Table 1: Electrical performance parameters of the fabricated $MoSe_2/ZrSe_3$ JFET devices.

Device Type	Transconductance (μS)	Mobility (cm^2/V)	Subthreshold Swing (V/dec)
$ZrSe_3/MoSe_2$(TG)	**12.8**	**366.95**	**13.25**
$ZrSe_3/MoSe_2$(BG)	7.46	215.83	16.49
$MoSe_2/ZrSe_3$(Gate)	0.238	161.23	1.94

The subthreshold swing (SS) was extracted from the steepest slope region of the semilogarithmic I_D-V_G transfer curve using the relationship SS = $d(V_G)/d(\log_{10} I_D)$. The calculation was performed over the gate voltage range where the drain current changes by at least two orders of magnitude, ensuring accurate determination of the switching characteristics.

Finally, we fabricated JFET devices based on $ZrSe_3$ and $MoSe_2$, and analyzed the characteristics of P-type and N-type JFETs, in which the materials served as either the gate and/or JFET channel. In the case of the P-type JFET, where $ZrSe_3$ was used as the channel material ($ZrSe_3/MoSe_2$), a maximum mobility of 366.95 $cm^2/V{\cdot}s$ was observed, which is higher than the 161.23 $cm^2/V{\cdot}s$ measured for the $MoSe_2/ZrSe_3$ N-type JFET. This enhanced mobility may be associated with differences in the transport properties and thicknesses of the $ZrSe_3$ and $MoSe_2$ channel materials. Moreover, in terms of subthreshold swing (SS), the P-type JFET exhibited a higher value of 13.25 V/dec compared to 1.94 V/dec for the N-type JFET. This difference is likely associated with differences in electrostatic gate coupling, interfacial trap states which affect the depletion behavior and gate controllability of the device. Additionally, the top and bottom gate configurations showed noticeable differences in electrical characteristics, with the top gate device exhibiting higher transconductance and mobility than the bottom gate device. This difference can be attributed to variations in the thickness of the $MoSe_2$ flakes used as the top and bottom gate contact materials, which may affect the gate coupling and contact resistance.

4 Conclusions

In conclusion, $ZrSe_3$ and $MoSe_2$ were obtained through mechanical exfoliation and transferred onto substrates, functioning as either the gate or the channel depending on the device structure. The electrical characteristics of JFET devices were analyzed and revealed that the JFET structure with $MoSe_2$ as the channel exhibited a mobility of 161.23 cm^2/V·s and a subthreshold swing (SS) of 1.94 V/dec. In the case of JFETs with $ZrSe_3$ as the channel, the top gate configuration exhibited superior performance, with a mobility of approximately 367 cm^2/V·s, whereas the bottom gate configuration exhibited a mobility of approximately 216 cm^2/V·s. This difference may be associated with variations in the thicknesses of the $MoSe_2$ gate flakes, which can affect gate coupling and contact resistance. For the $ZrSe_3$ channel JFETs, the SS values were 13.25 V/dec for the top gate configuration and 16.49 V/dec for the bottom gate configuration, both of which were higher than the SS value of 1.94 V/dec obtained for the $MoSe_2$ channel JFET. The findings discussed in the current manuscript suggest that precise control of the $ZrSe_3$ thickness during fabrication can significantly improve the electrical performance of the JFET devices. Furthermore, the results highlight the potential of heterojunction engineering involving $ZrSe_3$ and $MoSe_2$ in their two-dimensional forms for the development of future high-performance electronic devices [44], including high-electron-mobility transistors (HEMTs) and Hall-effect magnetic sensors.

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Author Contributions: The authors confirm contribution to the paper as follows: Conceptualization, Changlim Woo; methodology, Changlim Woo and Abdelkader Abderrahmane; validation, Pil Ju Ko and Abdelkader Abderrahmane; writing—original draft preparation, Changlim Woo; writing—review and editing, Pil Ju Ko and Abdelkader Abderrahmane; visualization, Changlim Woo and Pan Gum Jung; supervision, Pil Ju Ko. All authors reviewed and approved the final version of the manuscript.

Availability of Data and Materials: The data that support the findings of this study are available from the Corresponding Author, Pil Ju Ko, upon reasonable request.

Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest.

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